#3 Sheet 1 of 1

FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. NIT-201-02	SERIAL NO. 10/084,435
LIST OF DOCUMENTS CITED BY APPLICANT *(Use several sheets if necessary)*		APPLICANT N. KATOH et al	
		FILING DATE February 28, 2002	GROUP ~~2819~~ 2825

j1017 U.S. PTO 10/084435 02/28/02

U.S. PATENT DOCUMENTS

* EXAMINER INITIAL		DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE (If Appropriate)
PK	AA	5,774,367	06/30/98	Reyes et al	716	2	7/24/95
PK	AB	5,614,847	03/1997	Kawahara et al	326	98	8/24/94
PK	AC	6,118,309	09/2000	Akamatsu et al	327	108	5/22/97
PK	AD	6,222,410	04/2001	Seno	327	293	6/29/99
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

		DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
PK	AL	8-274620	10/18/96	Japan	H03K	19/094	Abstract ☐	☐
PK	AM	9-45785	02/14/97	Japan	H01L	21/82	Abstract ☐	☐
	AN						☐	☐
	AO						☐	☐
	AP						☐	☐

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, etc.)*

PK	AR		S. Mutoh et al, "1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS", IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. 30,
			No. 8, August 1995, pp. 847-854.
PK	AS		T. Sakata et al, "Subthreshold-Current Reduction Circuits for Multi-Gigabit DRAM's", 1993 SYMPOSIUM ON VLSI CIRCUITS DIGEST OF TECHNICAL PAPERS,
			May 1993, pp. 45-46.
	AT		

EXAMINER Phallaka Kik DATE CONSIDERED 5/15/03

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.